A Low Power Wideband 2.6GHz CMOS Injection-Locked Ring Oscillator Prescaler

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Abstract — **A high speed and low power prescaler based on injection-locked ring oscillator is presented. The proposed prescaler uses an adaptive biasing to increase the locking range and to eliminate the sensitivity of the locking phenomena to temperature and process variation. The designed circuit can be used in a fractional-N frequency synthesizer. Prescaler operates properly in temperature range of -20°C to +100°C and input frequency range from 2.2GHz to 2.6GHz in all process corners while its maximum power dissipation is 2mW at supply voltage of 1.5V.**

I. INTRODUCTION

In recent years, the wireless personal communication market has been growing explosively. Low cost and low power consumption are the key factors of success in this market. Frequency synthesizers as an essential part of any transceiver, in general, and VCO and prescaler as two main power consuming blocks in each synthesizer, in particular, have an important role in this respect.

In this paper we present the design of a low power prescaler based on injection-locked concept. Section II reviews general architecture of the proposed prescaler. In section III-A a simplified model for injection-locked frequency dividers is presented and capability of the circuit to have a wide locking range is proved. Section III-B is devoted to the design of two frequency dividers modulo-4 and modulo-2. Section III-C describes the design of an $\div 8/9$ prescaler and section III-D demonstrates how an adaptive biasing method could increase prescaler maximum operating frequency. The simulation results are presented in section IV and conclusions are made in section V.

II. PRESCALER ARCHITECTURE

Our proposed architecture consists of two cascaded fixed frequency dividers modulo-4 and modulo-2 followed by an $\div 8/9$ prescaler as shown in Fig. 1. The circuit is made of source-coupled logic (SCL) flip-flops and gates. Fully differential structure of the SCL results in low sensitivity to the common-mode noises such as substrate and supply noises. In addition, it can be connected directly to the VCO output without requiring any buffer. This results in less power consumption.

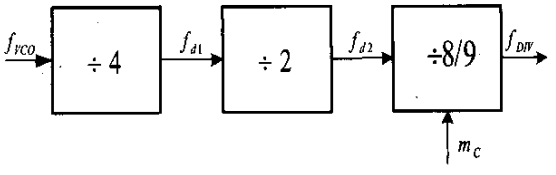

Fig. 1 General architecture of the proposed prescaler

The first block is an SCL D-flip flop with a negative feedback that can be looked upon as a ring oscillator. Its biasing has been selected to have a free-running frequency near to the one fourth of the input frequency. As a result, the first stage acts as a frequency divider by division factor of four. The $\div 8/9$ prescaler is a conventional one in which the SCL D-flip flop and gates are exploited to achieve the desired function

In this paper, each of the two first blocks is interpreted as a two-stage ring oscillator whose free running frequency is determined by the stage delay [1]. As it will be shown in the next section, by adjusting the load bias of each stage, we can achieve a free-running frequency near to the desired divided frequency. In principal, the circuit in Fig. 1 is a $\div 64/72$ dual modulus prescaler that can be used in a fractional-N frequency synthesizer whose fractional part has been multiplied by 8.

III. INJECTION LOCKED FREQUENCY DIVIDER

A. Injection-locked Frequency Divider Model

An injection-locked frequency divider is an analog divider that can be modeled as shown in Fig. 2 [2]. The signal with frequency f_i, whose frequency is to be

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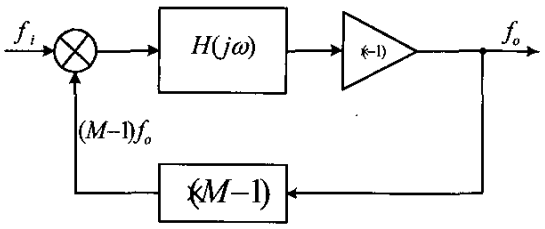

Fig. 2 An analog divider based on injection-locked

divided by the factor of *M*, and a postulated signal of frequency $(M\text{-}1)\,f_o$ are applied to the RF and LO ports of the mixer, respectively. The mixer output contains different sideband frequencies among which only the sideband $f_i - (M\text{-}1)\,f_o$ appears as the output. The low pass transfer function $H(j\omega)$ is the open loop frequency response of the ring oscillator. The functions of mixing and frequency multiplication in the feedback path are accomplished in the first stage of the oscillator.

In order to have a sustained oscillation, a total phase lag of 2π around the loop is required. This phase is provided through inversion (-1), $H(j\omega)$ and partially by the mixing action. It is also mandatory to have an open loop gain greater than unity at the oscillation frequency.

B .Fixed Frequency-Dividers Circuits

The same architecture is exploited for both fixed dividers but their bias values are different. Fig. 3 shows the block diagram of each divider that is a master-slave D flip-flop in a negative feedback loop.

The circuit can be interpreted as a two-stage ring oscillator in which each stage is consisted of a D-flip flop circuit as shown in Fig. 4 [3]. When a fixed bias is applied to the clock inputs (clk+, clk-), the circuit can be considered as a first order one and its frequency response will be as follows:

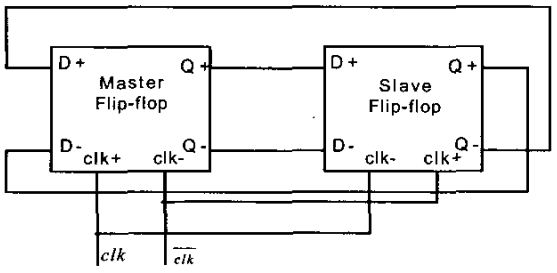

Fig. 3 Block diagram of a two-stage ring oscillator

$$H(j\omega) = A_o \frac{1 - j\omega/\omega_z}{1 + j\omega/\omega_P} \qquad (1)$$

Where A_o is the small signal dc gain of the stage, ω_P is a pole seen at the output due to the resistance of the pMOS load and that of the latch and the total capacitance at this node, and ω_z is a right-half plane zero (due to the drain-gate overlap capacitance of M1 and M2) that contributes a small negative phase shift. Therefore, at the limited free-running frequency ω_r, total phase shift of each stage is -90°. Two -90° lag phases and -180° phase shift through negative feedback connection across the stages provide required 360° phase shift for stable oscillation. By using (1) to write the system phase at ω_r, we obtain:

$$H(j\omega_r) = \tan^{+1}\left(\frac{\omega_r}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_r}{\omega_p}\right) \qquad (2)$$

On the other hand, we have $< H(j\omega_r) = -\pi/2$ which results in the following relation:

$$\omega_r^2 = \omega_p . \omega_z \qquad (3)$$

In addition to the phase condition, the system amplitude frequency response at ω_r must be greater than unity at the start of oscillation. Applying this condition to (1) and using the result in (3), yields in

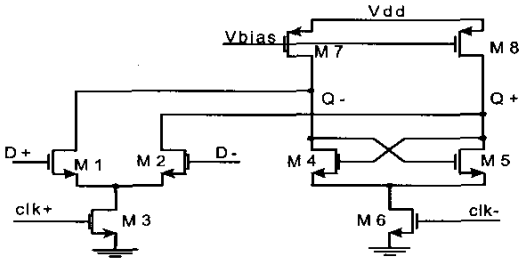

Fig. 4 Schematic of an SCL D-flip flop

greater than unity dc gain. (Ao > 1)

The circuit in Fig. 4 with injection signal applied to the gates of M3 and M6 can be modeled as a double balance mixer whose RF port is the gate of M3 (M6) and its LO port is the gate of M1 (M2). The circuit itself generates LO signal as mentioned before. Both fixed frequency dividers in Fig. 1 are comprised of the

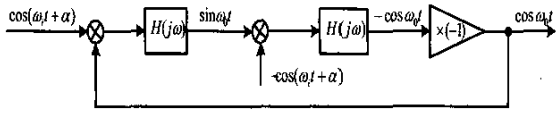

Fig. 5. Equivalent model of D-flip flop with injection signal

circuit shown in Fig. 3. Fig. 5 shows the equivalent model of the divider.

In Fig. 5, the two mixers model the nonlinearity of the differential pairs in the master and slave flip flops, respectively. The function of $H(j\omega)$ considers the low pass behavior of each block owing to the ω_P pole at the output. Inversion block is related to the reverse connection of the D-flip flop output to its input. The loop is supposed to have stable oscillation at frequency $\omega_o (\neq \omega_r)$, in that case phase condition calls for 360° total phase shift around the loop at ω_o. If ω_o is greater than ω_r, then the phase of $H(j\omega_o)$ is less than -90°. Since each stage should provide exactly -90° phase shift at ω_o, each mixer introduces extra positive phase θ to compensate for the stage excess phase lag. For ω_o less than ω_r stage phase at ω_o is less negative with respect to -90° and θ must be negative. The locking range of the divider is determined by the variation range of θ that can compensate the phase deviation of $H(j\omega_o)$ about -90°. The maximum range of θ depends upon to the amount of nonlinearity in the differential pair [1] and the ratio of the injection amplitude and the oscillation amplitude [4].

C. $\div 8/9$ *Prescaler design*

As shown in Fig. 6, the circuit consists of a synchronous SCL dual-modulus $\div 2/3$ prescaler followed by two divide-by-2 frequency dividers. A

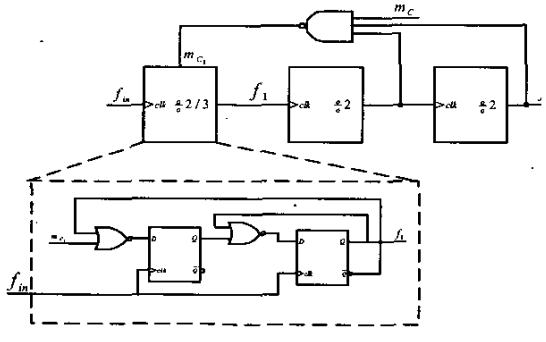

Fig. 6. Block diagram of the prescaler

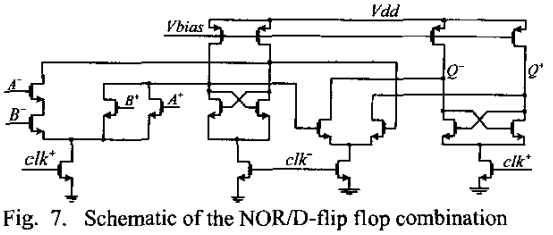

Fig. 7. Schematic of the NOR/D-flip flop combination

NOR/D-flip flop combination [5] is used in $\div 2/3$ prescaler as depicted in Fig. 7. The structure of the divide-by-2 circuit is similar to that used in the modulo-4 and modulo-2 injection-locked dividers with different bias.

D. *Biasing Circuit*

The locking range of an injection-locked divider is small in comparison to its free running frequency. On the other hand, this frequency depends greatly upon process and temperature. Therefore, temperature and process variations may violate the locking condition.

In this section, a bias circuit is described which maintains the divider in locking state in spite of these variations. The main idea used to reach this objective is to change the Vbias in Fig. 4 proportional to temperature and process to keep tight the free-running frequency about its typical value. Fig. 8 shows the schematic of the divider bias circuit.

For a constant current Io, Vg varies proportionally with temperature and process. The difference of Vg and a fixed bandgap voltage reference Vref is amplified by a differential pair and converted to an equivalent current Iax. This current adjusts the total bias current to compensate the changes in the free-running frequency due to temperature and process variations.

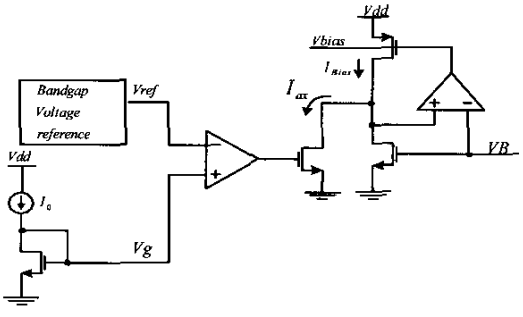

Fig. 8. Bias circuit for frequency divider

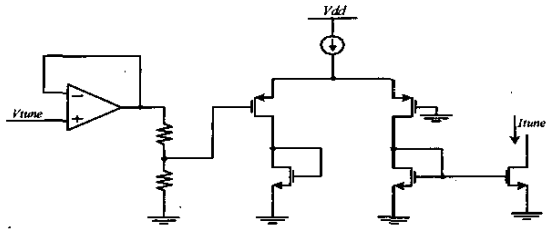

Fig. 9 Auxiliary bias circuit for tracking input frequency

If the divider input frequency varies in a limited range, it should also be considered in the bias circuit to keep the divider locked. This condition occurs, for example, in a frequency synthesizer in which the divider input frequency is subject to changes due to the variation of the VCO output frequency. For this purpose we can use the VCO tuning voltage to change Vbias so that the divider free-running frequency can tack its input frequency and divider will remain in the locked condition. Fig. 9 shows the used circuit for this purpose.

IV. SIMULATION RESULTS

The prescaler simulation was carried out for different process corners of 0.24 μm CMOS technology, in a temperature range of -20°C to +100°C, and for the input frequencies from 2.2GHz to 2.6GHz in order to evaluate the ability of the circuit to perform the correct division. Modulus control of the ÷8/9 prescaler was selected as a random sequence of high and low levels with minimum time duration of 56 ns. The divide-by-4 injection-locked frequency divider has been used as a first stage in prescaler. This results in great reduction in power consumption of the whole prescaler. The

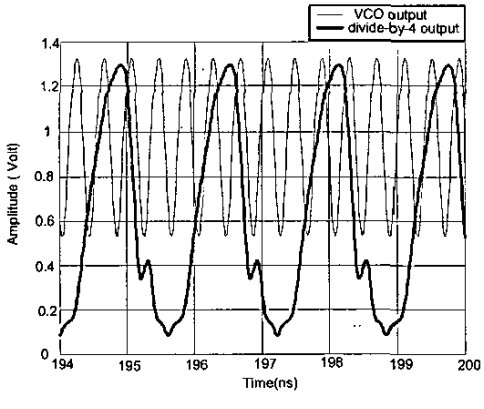

Fig. 10 Input and output waveform of the first ILFD

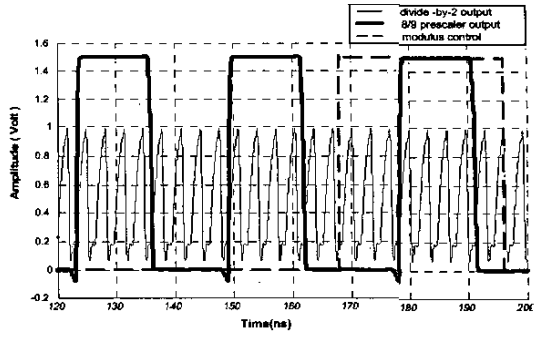

Fig. 11 Outputs of divide-by-2, 8/9 prescaler, and modulus control

modulo-4 divider, modulo-2 divider, ÷8/9 prescaler and bias circuit consume 370μA, 208μA, 395μA, and 318μA, respectively from a 1.5-V supply. Fig. 10 shows the input and output waveforms of the first fixed divide-by-4 stage. The output waveforms of the second stage (divide-by-2), ÷8/9 prescaler and modulus control signal are shown in Fig. 11.

V. CONCLUSION

A 64/72 prescaler was designed. Its power consumption can be considerably reduced by exploiting the injection-locked ring oscillators as fixed dividers in the first stage of the prescaler. An adaptive biasing technique was applied to provide sufficient operation bandwidth for the prescaler.

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