Homework #2
(تاریخ تحویل ۱۹ فروردین ماه)

- Design and size : $F=\overline{((A\&B)+(C\&D))\&E}$
  - Design NMOS pull down network
  - Design PMOS pull up network
  - Size NMOS, as unit size
  - Size PMOS according to NMOS network
  - Using 32nm Technology, run a SPICE simulation and verify your design's operation