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Mir Bintul Islam (

mir1909967@st.jmi.ac.in)

Jamia Millia Islamia

M. Nizamuddin

Jamia Millia Islamia

Research Article

Keywords: Carbon allotropes, CNTFET, GNRFET, operational transconductance amplifier

Posted Date: September 21st, 2022

DOI: https://doi.org/10.21203/rs.3.rs-2063314/v1

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Design of Folded Cascode Operational Transconductance Amplifiers (FC-OTA) based on Carbon Allotropes and their Comparative Analysis

Mir Bintul Islam^{1*} M. Nizamuddin²

¹PhD Scholar, Electronics and Communication Engineering Department, Jamia Millia Islamia, New Delhi 110025, India

²Professor, Electronics and Communication Engineering Department, Jamia Millia Islamia, New Delhi 110025, India

Abstract

In this work, a folded cascode operational transconductance amplifier using CNTFET and GNRFET has been designed and simulated using HSPICE software. The structures of FC-OTA are formed using pure CNTFET and its hybrids which involve combination of CNTFET and CMOS both and lastly a structure has been formed using GNRFET. The detailed study reveals that compared to conventional CMOS-based FC-OTA, the performance of CNTFET- based FC-OTAs shows a lot of improvement. An appreciable increase in dc gain, output resistance and CMRR is observed in CNT based FC-OTA as compared to conventional CMOS-based FC-OTA. The phase margin (PM) and gain margin (GM) obtained in CNT- based FC-OTAs shows that they are quite stable. In addition, GNRFET-FC-OTA was also simulated and compared with CNTFET-FC-OTA. On comparison, it showed that CNT-based device showed significant increase in dc gain compared to GNRFET-FC-OTA. The performance of proposed FC-OTAs was further studied by changing CNT diameter, CNT pitch and no of CNTs and it was observed that by using optimized values for these parameters, the performance of proposed FC-OTA can be improved significantly. To sum up, it was observed that folded cascoded technique has significantly increased the gain in CNTFET-based FC-OTAs.

Keywords: Carbon allotropes, CNTFET, GNRFET, operational transconductance amplifier

1. Introduction

The operational transconductance amplifier (OTA) plays a significant part in countless analog and mixed-signal integrated circuits like data converters, modulators, variable-gain amplifiers, continuous time oscillators, interface circuits and filters [1-3]. OTA offers flexibility and tunability owing to an extra control input, large dynamic range, large bandwidth and no excess phase issues in comparison to an OP-AMP [4-6]. Hence, it widens its application area compared to conventional OP-AMP devices [7-9]. Even so, in submicron technology nodes, an OTA suffers

^{*}Corresponding Author Email: mir1909967@st.jmi.ac.in

from speed and gain degradation [10-12]. The gain degradation issue in nano-scale regime will be a notable snag in realizing highly dense integrated circuits [11-13].

In order to overcome the problems of gain degradation in OTAs, many methods have been used but the cascoding technique has shown notable improvement in gain degradation problem in such devices [14-16]. The cascoding technique plays an important role in improving the output resistance thereby increasing the DC gain and also reduced miller capacitance which leads to improved bandwidth. Despite the fact that cascoded OTAs have improved gain but power dissipation and speed are still important issues that need to be addressed [18]. Another important configuration of cascoded OTAs is folded cascode OTA (FC-OTA) which gives large bandwidth, high voltage swing, better frequency response and high gain. Meanwhile, FC-OTA also faces large power consumption issues that prevent its large integration realization and leads to its degradation [16-19].

The problems of scaling and power dissipation in FC-OTAs can be fixed by using carbon nanotube field effect transistors (CNTFET) in place of MOSFET [20-25]. In comparison to conventional MOSFET, a CNTFET based device has low power consumption and reduced short channel effects and it also shares same fabrication scheme as conventional MOSFET.

In this work, CNTFET based FC-OTAs have been designed and simulated using HSPICE software at 45nm technology node. For simulation of CNTFETs Verilog-A Stanford model has been used and for conventional n and p channel MOSFETS BSIMv4.6.1 Berkeley Predictive Technology model at 45nm technology node has been used [26]. Three types of CNT-based FC-OTAs which include (a) pure CNT-FC-OTA which uses CNT-based NMOS and PMOS transistors, (b) NCNTFET-PMOS-FC-OTA which uses CNT-based NMOS and conventional PMOS transistors, (c)PCNTFET-NMOS-FC-OTA which CNT-based PMOS and conventional NMOS transistors have been designed and compared with conventional CMOS-based FC-OTAs. Also, in the end, a 32nm technology node pure CNTFET-FC-OTA has been simulated and compared with 32nm pure GNRFET-FC-OTA.

2. Theoretical Background

The carbon based FETs used in this work are CNTFET and GNRFET which have been simulated using HSPICE and are briefly overviewed.

2.1 Carbon nanotube field effect transistor (CNTFET)

Carbon nanotubes (CNTs) are an allotrope of carbon and were discovered by Dr. Sumio Iijima in 1991 [27]. CNTs can be either single-walled CNTs (SWCNTs) or multi-walled CNTs (MWCNTs) as shown in the Fig 1 (a). SWCNTs contain only one graphene cylinder whereas more than one graphene cylinder is present in MWCNTs. CNTs exhibit some of the unique electrical properties and exceptional strength which offers them diverse applications in optics, nanotechnology, electronics and various other fields.

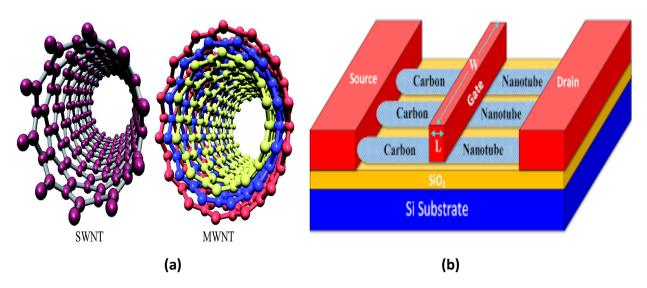


Figure 1: (a) SWNT and MWNT (b) Schematics of CNTFET

The schematics of a typical CNTFET is illustrated in Fig. 1 (b) [28]. CNTFET is a four terminal device consisting of gate, source, drain and substrate, similar to traditional MOSFET. CNT channel region is undoped, and acts as both the source/drain extension region and/or interconnects between two adjacent devices whereas the source and drain regions of the CNTFET are heavily doped like in conventional MOSFET [29]. The CNTFET channel's turn ON and OFF characteristics are controlled by the gate. The threshold voltage (V_{th}) of intrinsic CNT channel can be calculated using chirality vector as [30]:

$$Vth = \frac{aV\pi}{\sqrt{3qDcnt}} \cong \frac{0.43}{Dcnt(nm)} \tag{1}$$

Where a = 2.49 Å, q = unit electron charge, Dcnt = diameter of the CNT and $V\pi$ = carbon π - π bond energy [31] .The diameter of CNT can be calculated using the following equation:

$$Dcnt = \frac{\sqrt{3a}}{\pi} \sqrt{n^2 + m^2 + m^2} \tag{2}$$

The operating characteristics of CNTFET are similar to MOSFET. Just as in the case of other FETs, CNTFET also relies on its gate terminal to modulate carrier concentration in the channel by applying a field perpendicular to charge flow between sources and drain terminal [30]. The carrier transport between the drain and source takes place through CNTs and is ballistic in nature. Ballistic transport of charge carriers mean that the mean free path is longer than the dimensions of the device. Hence, the charge carriers do not collide which reduces resistance to negligible levels, resulting in higher mobility as compared to bulk MOSFETs [32]. Since the current driving capability with same geometries is equal in CNTFET technology, so in order to match the devices a ratio of '1' can be easily used for p-type(P-CNTFET) and n-type(N-CNTFET) devices to design the circuits unlike CMOS technology. Also, contrary to CMOS where widths and lengths are changed

to adjust the PMOS/NMOS ratio, a CNTFET based circuit is designed in terms of following parameters [30]:

- 1. Diameter of CNT (D_{CNT}): It is directly related to threshold voltage of device so it should be chosen very carefully.
- 2. Number of CNTs (N): It is important to determine number of CNTs in order to ensure sufficient current supply for driving fixed capacitive loads.
- 3. Inter-CNT Pitch (S): It is an important factor affecting the performance of CNTFET and is defined as the distance between the centers of two adjacent CNTs in the channel.

2.2 Graphene Nanoribbon Field Effect Transistor (GNRFET)

Graphene is a zero-bandgap material, formed of a single sheet of carbon atoms packed in a 2D honeycomb lattice. Figure 2 shows the MOSFET-type GNRFET structure used in our work. Each GNR is intrinsic (undoped) under the gate and heavily doped with doping fraction f_{dop} between the wide contact and the gate. The intrinsic part is called the channel and the doped parts are known as reservoir. The channel is made up of parallelly arranged graphene nano-ribbons mainly of arm-chair chirality and the channel is turned on and off by the gate. The channel width is given by [33]:

$$WGNR = nrib \cdot (Wsp + 2 \cdot Wch)$$

Where, W_{GNR} is the gate width, n_{rib} is the number of nanoribbons, W_{sp} is the spacing between the nanoribbons, and W_{CH} is the nano-ribbon width given by $\sqrt{3}d_{cc} \cdot (N+1)/2$, where N is the number of dimer lines and d_{cc} is the carbon-carbon bond distance [33]

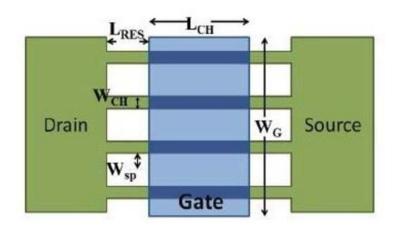


Figure 2: Illustration of GNR-FET [34]

3. Methodology

An operational transconductance amplifier (OTA) is actually a voltage controlled current source (VCCS) device and is a prime unit in analog as well as mixed digital-analog circuits [35]. The prime advantages of an OTA are tunability and flexibility which are realized by external bias current I_{abc} and hence it widens its application domain over conventional OP-AMP.

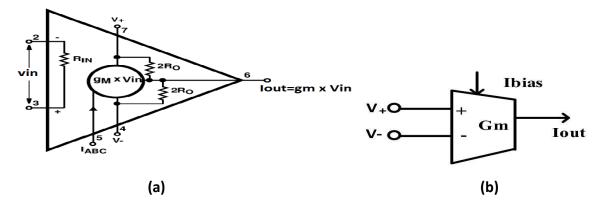


Figure 3: (a) Equivalent circuit and (b) symbol of an OTA

Figure 3 shows the equivalent circuit and symbol of an OTA. An ideal OTA has infinite output resistance. The output current i_0 of an OTA is given by equation (3)

$$i_0 = g_m (v_p - v_m) \tag{3}$$

where, v_p and v_n are positive and negative terminals and g_m is the transconductance.

In this work three CNT- based FC-OTAs have been designed and compared with conventional CMOS-FC-OTA. The proposed CNTFET-based FC-OTAs have been designed using Stanford CNTFET model at 45nm technology node in HSPICE software [36]. The conventional CMOS based FC-OTA and CNT based FC-OTA circuits are shown in fig 4. In case of PCNT-NMOS-FC-OTA, it uses p-CNTFETs as sinks and conventional NMOS transistors as source whereas in case of NCNT-PMOS-FC-OTA n-CNTFETs it uses n-CNTFETs as sinks and conventional PMOS as source. All the FC-OTAs are designed using 0.9V at 45technology node in HSPICE. The Stanford university CNTFET model used is a SPICE-compatible compact model which describes enhancement mode, unipolar MOSFETs with single walled CNT as channels. The model is based on quasi-ballistic transport and accounts for several practical non-idealities like scattering of charge carriers due to acoustic and optical phonons in the nanotubes, various parasitic capacitances, the gate-to-gate and gate-tocontact-plug capacitances, charge screening effect among adjacent nanotubes, surce/drain resistances and band-to-band leakage current [10,18,37]. The CNTFETs fabricated have Pd source/drain contacts, Al gate contact, intrinsic device capacitance (2-5aF/nanotube) and overlap and fringe capacitances (~0.1fF/nanotube). The other parameters included in the simulation study are physical channel length (Lch) of 45nm, mean free path in CNT (Lgeff) of 200nm, gate oxide dielectric constant of 16, gate oxide thickness (Tox) of 4nm, Fermi level of the doped S/D tube of 0.6eV, coupling capacitance of 40Pfm⁻¹ and a CNT work function of 4.5 [10,17]. The

proposed folded cascode OTAs have a differential input pair consisting of n-type transistors. Owing to greater mobility in case of N-type device, P-type input differential pair will offer a lower transconductance than N-type pair. Thus, NCNTFET has been chosen in order to ensure largest gain possible.

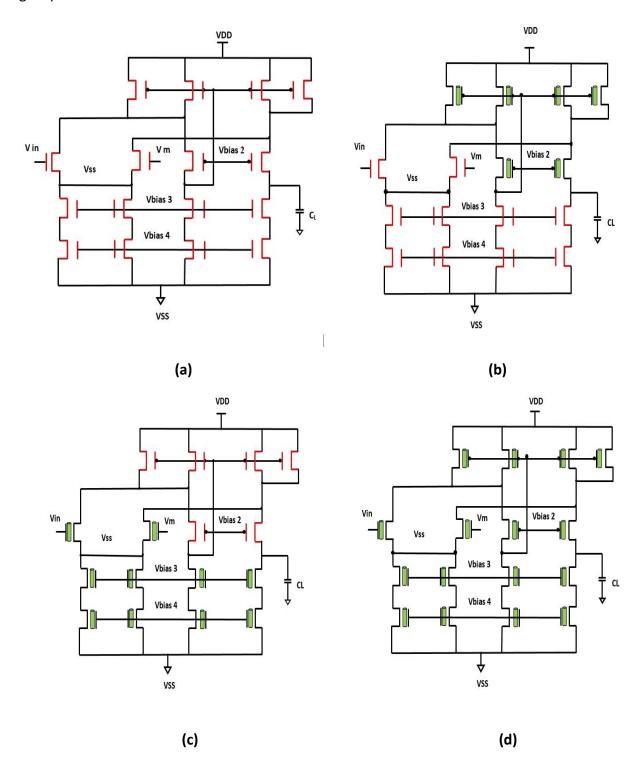


Figure 4: FC-OTAs designed and simulated (a) Bulk CMOS-FC-OTA (b) PCNT-NMOS-FC-OTA (c) NCNT-PMOS-FC-OTA (d) pure CNT-FC-OTA

4. Results and Discussion

The results for the effect of variation in CNT parameters on the proposed OTAs along with the stability analysis have been shown and discussed. A comparative analysis has also been carried out between pure and hybrid FC-OTAs at 45nm technology node and another comparative analysis has been done between pure CNTFET-FC-OTA and pure GNRFET-FC-OTA at a technology node of 32nm.

4.1 Effect of variation of number of CNTs (N) on the performance of the proposed FC-OTAs

The results show the effect of increasing the number of CNTS (N) on various performance measuring parameters of the proposed CNT-based FC-OTAs. It indicates that the N has an important part in optimizing the total performance of the proposed FC-OTAs. Increasing N increases the current carrying capability of a CNTFET because a single CNT carries a constant current due to fixed S. Figure 5 shows the effect of N on various parameters like dc gain, bandwidth, output resistance and average power. Fig 5 (a) shows that with the increase in N, the DC gain of all the CNT-based FC-OTAs increases slightly and later on saturates. Of all the FC-OTAs, pure CNT-FC-OTA has the highest gain in comparison to hybrid FC-OTAs because of the presence of PCNTFETs and NCNTFETs which have higher transconductance and driving capability in comparison to conventional bulk MOSFETs. An equation between CNTFET ON current and N, which shows that on increasing N, the driving capability of CNTFETs increases significantly is given as [10, 24, 25]:

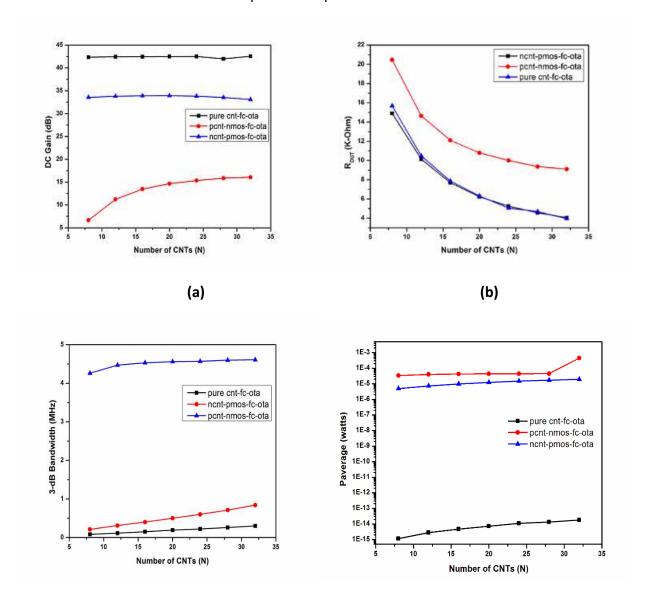
$$I_{\text{CNTFET}} \approx N \, g_{\text{CNT}} \, (V_{\text{DD}} - V_{\text{th}}) / \, (1 + g_{\text{CNT}} \, L_{\text{s}} \, \rho_{\text{s}}) \tag{4}$$

Where I_{CNTFET} is the ON current of CNTFET, g_{CNT} is the transconductance per CNT, L_s is the source length (doped CNT region), ρ_s is the source resistance per unit length of doped CNT. The DC gain increases slightly and then saturates owing to the screening effect caused by large number of adjacent CNTs [22, 24, 38, 39, 40] in the channels of both hybrid and pure CNT-OTAs. The effective channel width (W_{eff}) of a CNTFET is given by the equation:

$$Weff = N * DCNT * a (5)$$

Where α is the screening effect coefficient (0 < α < 1). For N = 1, the screening coefficient α is 1 and for N > 1 its value is also less than 1. Among the hybrid FC-OTAs, the NCNT-PMOS-FC-OTA has a larger gain compared to PCNT-NMOS-FC-OTA. This can be attributed to larger transconductance in NCNT-PMOS-FC-OTA because of more number of CNTFETs in NCNT-PMOS-FC-OTA (10 n-CNTFETs) than in PCNT-NMOS-FC-OTA (6 p-CNTFETs). Fig 5 (b) shows that with the increase in number of CNTs, the output resistance (R₀) decreases in all the FC-OTAs. The increase in N leads to an increase in the width, so output resistance will decrease with increase in N. Fig 5

(c) shows that with the increase in N, the bandwidth of all the devices will increase. The main problem faced by CNT- based devices is low bandwidth which is evident from the figure as pure CNT-FC-OTA has the lowest bandwidth among all the devices. This can be ascribed to the use of high dielectric constant gate oxide in CNTFET. The bandwidth reduction occurs due to significant increase in gate capacitances in the CNTFETs [10, 41]. PCNT-NMOS-FC-OTA has the highest bandwidth due to better switching of NMOS and p-CNTFETs. Fig 5 (d) shows the effect of increasing N on the average power consumption of CNT- based FC-OTA. Average power increases with the increase in N and it is again due to increment in drive capability of CNTFETs on increasing N. But the average power dissipation in pure CNT-FC-OTA is very less due to small resistance in the CNT channel, 1D ballistic transport, reduced parasitic capacitance and reduced leakage in pure CNT-FC-OTA [39, 42]. Power dissipation in PCNT-NMOS-FC-OTA in case of hybrid FC-OTAs is slightly higher than NCNT-PMOS-FC-OTA which could be mainly due to low drive current in NCNT-PMOS-FC-OTA and as a result lower power dissipation.



(c) (d)

Figure 5: Effect of variation of CNT number on (a) DC gain (b) output resistance (c) 3-dB bandwidth (d) average power in proposed FC-OTAs

4.2 Effect of variation of CNT diameter (D_{CNT}) on the performance of the proposed FC-OTAs

It has been observed that by optimizing the CNT diameter, the performance of the proposed FC-OTAs can be further improved. Fig 6 shows the effect of increasing CNT diameter on various performance measuring parameters. Fig 6 (a) shows that with the increase in CNT diameter, the DC gain of CNT based OTAs decreases. This can be mainly due to the fact that with the increase in CNT diameter, R₀ increases which leads to an increase in screening and scattering effects and as a consequence it deteriorates the gain. Further PCNT-NMOS-FC-OTA has the lowest gain of all mainly because of less number of CNTFETs (p-CNTFET) used as source and more number of conventional MOSFETs (NMOS) used as sink as compared to NCNT-PMOS-FC-OTA. Fig 6 (b) shows the variation of output resistance with increase in CNT diameter. The increase in D_{CNT} increases the transconductance which increases the output current and thereby decreasing the output resistance [41, 43, 44]. Fig 6 (c) shows that with the increase in CNT diameter, the 3-dB bandwidth of CNT-based FC-OTAs also increases. This can be associated with decrease in the parameter R₀ upon increase in D_{CNT} given by the equation (6) [24, 41]

$$f_{3-dB}=1/2\pi R_0 C_L \tag{6}$$

Among the hybrid FC-OTAs, the increase in bandwidth is more pronounced in NCNT-PMOS-FC-OTA in comparison to both PCNT-NMOS-FC-OTA and pure CNT-FC-OTA. The small drive current is the main reason for poor bandwidth in NCNT-PMOS-FC-OTA for small diameter. But as the diameter increases in CNT, both bandgap and threshold voltage will decrease which will raise the drive current and as such the bandwidth will increase. This reason holds true for PCNT-NMOS-FC-OTA and pure CNT-FC-OTA. Figure 6 (d) shows the variation of power dissipation with increasing D_{CNT} . The bandgap decreases with the increase in D_{CNT} , which reduces the threshold voltage and thereby, increasing the leakage and static power dissipation [10, 39, 40, 44]. The change in bandgap with respect to D_{CNT} is given by the equation (7) [10, 39].

$$Bandgap = 0.8eV / D_{CNT}$$
 (7)

The average power increase with respect to increase in D_{CNT} is least in case of pure CNT-FC-OTA due to 1D ballistic transport and reduced parasitic capacitance.

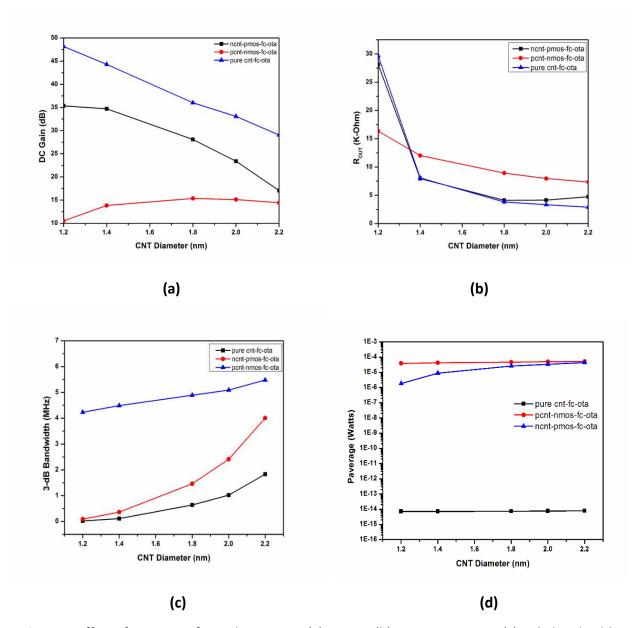


Figure 6: Effect of variation of CNT diameter on (a) DC gain (b) output resistance (c) 3-dB bandwidth (d) average power in the proposed FC-OTAs.

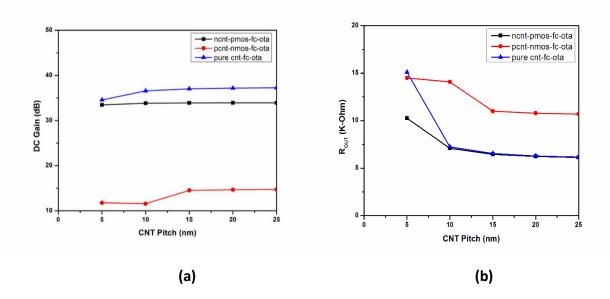
4.3 Effect of variation of inter-CNT pitch (S) on the performance of the proposed FC-OTAs

The separation between the centers of two adjacent CNTs in CNTFET known as pitch (S) also plays an important role in determining the performance of CNT based devices. For a fixed N=20 and $D_{CNT}=1.5$ nm, the variation of CNT pitch on various performance measuring parameters like dc gain, output resistance , bandwidth and power dissipation in CNT based devices have been studied. Changing the separation between the adjacent CNTs play a significant role in change in

all important performance measuring parameters and it has been observed that CNTs will carry an identical current for S larger than 20nm and for smaller values of S the drive current and gate capacitance of CNTs in the middle will be smaller compared to CNTs at the edges due to screening effects by adjacent CNTs [10, 41]. Fig 7 (a) shows that pure CNT-FC-OTA has the highest gain among all and with increase in S the gain initially increases but then saturates. The reason can be due to increase in transconductance which increases the dc gain. The saturation of dc gain can be attributed to increase in inter-CNT screening effect which decreases drain current and net gate capacitance and hence leads to saturation of dc gain [10, 41]. The change in channel width (W) with respect to S is given in the equation (8)

$$W = (N-1) S + D_{CNT}$$
(8)

In case of hybrid FC-OTAs, the dc gain of NCNT-PMOS-FC-OTA is more as compared to PCNT-NMOS-FC-OTA. Fig 7 (b) shows the variation R₀ with increasing S. With increase in S, channel width increases which in turn increases output current and hence decreasing output resistance [23, 24, 25]. Fig 7 (c) give the bandwidth of FC-OTAs and it can be observed that bandwidth increases in all the devices with an increase in S and hybrid FC-OTAs have better bandwidth than pure CNT-FC-OTA because hybrid FC-OTAs carry bulk transistors which have reduced capacitances that CNTFETs and as such have greater bandwidth than pure CNT-FC-OTA. Fig 7 (d) shows the average power dissipation. As S increases, the average power initially increases but then saturates upon further increase in S. The average power in pure CNT-FC-OTA is least.



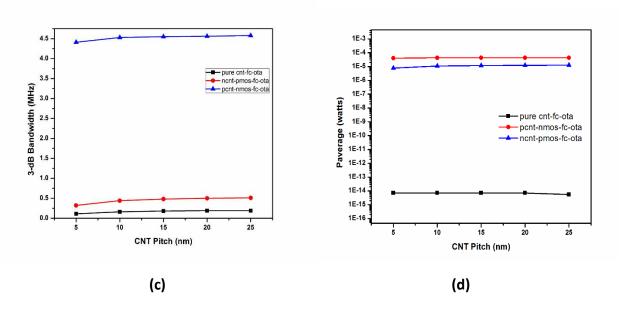
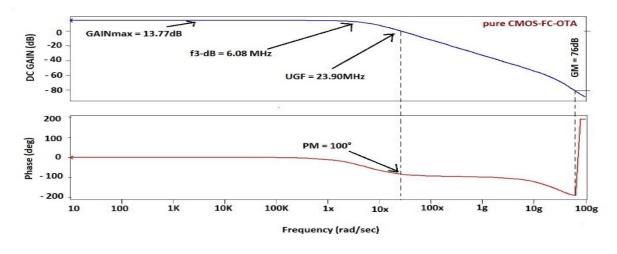


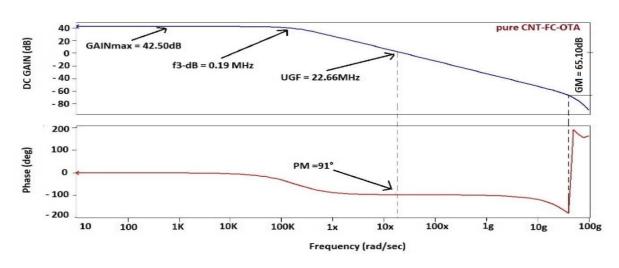
Figure 7: Effects of variation of CNT pitch (S) on (a) DC gain (b) output resistance (c) 3-dB bandwidth (d) average power in the proposed FC-OTAs

4.4 Stability analysis of the proposed FC-OTAs

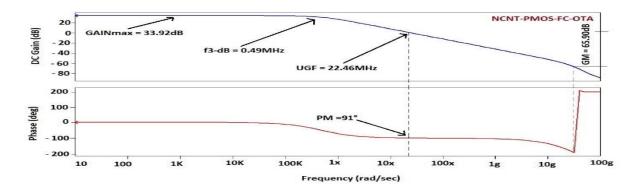
The gain and phase margins of the proposed pure CNT-FC-OTA, hybrid FC-OTAs and bulk CMOS FC-OTA have been observed to analyse the stability of the devices. For a stable system, the phase margin should be minimum 45°, although a 60° phase margin is more acceptable [4, 5]. On observing the values of phase and gain margins of all the designed FC-OTAs it can be said that they are all quite stable. The phase and gain margin for pure CNT-FC-OTA is 91° and 65dB respectively. The hybrid FC-OTAs are also stable with a phase and gain margin of 101° and 73dB for PCNT-NMOS-FC-OTA and phase and gain margin of 91° and 65dB for NCNT-PMOS-FC-OTA respectively. The phase and gain margin of bulk CMOS based FC-OTA are 100° and 76dB respectively and are shown in the figure 8. The unity gain frequency (UGF) is also shown in the figure 8 which is 23.90MHz for pure CMOS-FC-OTA and 22.66MHz for pure CNT-FC-OTA.



(a)



(b)



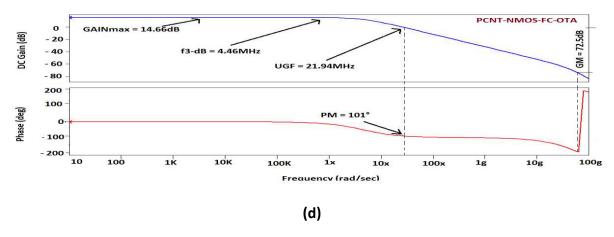


Figure 8: Gain and phase margins of (a) pure CMOS-FC-OTA (b) pure CNT-FC-OTA (c) NCNT-PMOS-FC-OTA (d) PCNT-NMOS-FC-OTA

4.5 Comparative analysis of pure CNT-FC-OTA, hybrid FC-OTAs and the CMOS based FC-OTA.

Table 1 gives the performance analysis of the proposed FC-OTAs designed and simulated in this work. The comparisons have been made using similar biasing and sizing conditions. The proposed circuits are based on 45nm technology node and use VDD=0.9V and C_L=1pF. The table shows that pure CNT-FC-OTA has the highest gain and CMRR, which can be attributed to large transconductance, high driving capability and quasi-1D ballistic transport; whereas CMOS-FC-OTA has the lowest gain of all and the gain of hybrid FC-OTAs lies between the gain of pure CNT-FC-OTA and pure CMOS-FC-OTA. The conventional CMOS-FC-OTA has the highest bandwidth of all whereas low bandwidth is the downside of CNT-FC-OTA which is due to high output resistance in pure CNT-FC-OTA.

Table 1: Performance comparison of CNTFET, hybrid and bulk FC-OTA at $C_L = 1$ pf, $V_{DD} = 0.9$ V, N=20, S=20 nm, $D_{CNT} = 1.5$ nm @ 45 nm technology node

S.No	Parameters	CMOS-FC-OTA	NCNT-PMOS-	PCNT-NMOS-	Pure CNT-FC-
			FC-OTA	FC-OTA	ОТА
1.	DC Gain (dB)	13.77	33.92	14.66	43.50
2.	Bandwidth (MHz)	6.09	0.49	4.56	0.19
3.	R _O (KΩ)	4.68	6.23	10.79	6.31
4.	Phase margin in deg	100	91	101	91
5.	Gain margin in deg	76	65	73	65
6.	U.G.F (MHz)	23.90	22.46	21.94	22.66
7.	Average power	70.59μw	12.20μw	43.42μw	7.14fw
8.	CMRR	53.63	68.43	53.80	73.51

4.6 Comparative analysis of pure CNTFET-FC-OTA and pure GNRFET-FC-OTA.

The same circuit blocks are designed using 32nm technology node to form pure CNTFET-FC-OTA and pure GNRFET-FC-OTA. Lastly, the two designs are compared in terms of a number of circuit parameters. Table 2 gives the performance analysis of the pure CNTFET-FC-OTA and pure GNRFET-FC-OTA designed and simulated in this work. The both proposed circuits are based on 32nm technology node and use VDD=0.9V and C_L =1pF. In case of GNRFET, the simulation is performed with parameters set as N=12, f_{DOP} = 0.001, thickness of oxide=0.95nm, no of nanoribbons is kept 6 and W_{sp} =2nm. As can be seen from the table the circuit parameters of CNTFET- based devices are better in comparison to GNRFET devices mainly due to the fact that CNTFET provides better I_{ON}/I_{OFF} ratio, smaller sub-threshold swing and higher transconductance in comparison to GNRFET [45]. Also, unlike nanoribbons, CNTs are immune to edge defects which is an important aspect of CNTs [46]. The bandwidth of CNTFET is low as compared to GNRFET which is its major drawback that needs to be taken care of.

Table 2: Performance comparison of pure GNRFET-FC-OTA and pure CNTFET-FC-OTAs at $C_L = 1$ pf, $V_{DD}=0.9$ V @ 32 nm technology node

S.No	Parameters	Pure CNTFET-FC-OTA	Pure GNRFET-FC-OTA
1.	DC Gain (dB)	76.90	13.50
2.	Bandwidth (MHz)	0.004	1.85
3.	R _O (ΚΩ)	5.32	14.61
4.	Phase margin in deg	89.97	102
5.	Gain margin in deg	75.98	88.7
6.	U.G.F (MHz)	27.12	7.96
7.	Average power	3.53fw	0.2uw
8.	CMRR	85.18	40.31

5. Conclusion

In this work, folded cascode operational transconductance amplifiers based on CNTFET and GNRFET have been discussed. In case of CNT-based FC-OTAs, three types which were pure CNTFET-FC-OTA and its two hybrid FC-OTAs were designed and tested using HSPICE software at 45nm technology. The important parameters were simulated and then compared with the conventional CMOS-based OTAs. The performance of CNT-based FC-OTAs was significantly enhanced as compared to CMOS based FC-OTAs. The parameters like dc gain, output resistance and CMRR showed improvement and also the power consumption was less compared to CMOS-FC-OTA. In addition, the impact of changing various parameters of CNT like diameter, no of tubes, CNT pitch on important performance measuring parameters was also studied revealing the importance of changing every parameter in circuit simulation. Further, a comparative analysis of pure CNTFET-FC-OTA has been made with pure GNRFET-FC-OTA at 32nm technology in HSPICE. It is well observed that folded cascode technique has significantly increased gain in CNTFET-based FC-OTAs.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Ethics Statement

This work is the authors' own original work, which has not been previously published elsewhere.

Data Availability Statement

All data included in the study are available upon request by contacting the corresponding author.

Funding Statement

Not Applicable

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