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A novel SOI-MESFET with symmetrical oxide boxes at both sides of gate and extended drift region into the buried oxide

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ABSTRACT

In this paper a novel structure for silicon on insulator metal semiconductor field effect transistors (SOI MESFETs) is proposed. The proposed structure contains two symmetrical oxide boxes at both sides of gate metal and extended drift region into the buried oxide which is named SO-ED-SOI-MESFET. SO-ED stands for symmetrical oxide boxes and extended drift region. DC and radio frequency characteristics of the SO-ED are analyzed by 2-D numerical simulation and compared with conventional SOI MESFET (C-SOI MESFET) characteristics. The obtained results demonstrate the superiorities of the proposed structure over C-SOI MESFET including increased breakdown voltage, higher driving current and improved RF characteristics. The extended drift region improves the current capability by increasing the effective channel thickness. The oxide region boosts the breakdown voltage due to its high tolerable electric field. Also, RF performance of the device is enhanced because of modified gate-source and gate-drain capacitances in the proposed structure. Unilateral power gain, maximum available gain and current gain experience 63, 52 and 63.5% improvement by applying the proposed structure, respectively. Thus the proposed structure can be considered as a proper candidate for using in high power and high frequency applications.

1. Introduction

Nowadays, silicon-on-insulator (SOI) technology is gaining more attention as a worthy technology in very large scale integration (VLSI) circuits due to its advantages over other technologies, including lower parasitic capacitances, higher speed, and lower leakage current [1–3]. SOI metal-semiconductor field-effect transistor (SOI-MESFET) is one of the most noticeable transistors based on SOI technology because of its significant features like being compatible with conventional CMOS processing and having high frequency parameters [4,5]. SOI MESFET has higher carrier mobility in the channel as compared to the SOI MOSFET. This property has significant consequences and enhances the performance of the device. For instance, high carrier mobility results in high transconductance and therefore high driving current. It also influences RF characteristics of the device and leads to higher transit frequencies [6–8]. Based on proper capability of SOI devices in high voltage and RF applications, many studies have been conducted on these devices. This studies include some aspects such as modeling, proposing different applications for these devices, and making some changes in the conventional structure to present novel structures and enhance their performance [7–13].

Precious features of SOI MESFET enable it to be used in high power applications, military communications, telecommunication cellular base stations, satellites, aerospace, and data storage [14–16]. These devices beside high electron mobility transistors (HEMTs) [17,18] have been widely considered in RF and high power applications. Therefore device researchers have tried to propose new structures for SOI MESFET in order to enhance their characteristics like maximum oscillation frequency, cut-off frequency, power gains and current gain [19–24]. These structures include some advantages and disadvantages. For example, a recently reported structure POML [24], shows high breakdown voltage and maximum oscillation frequency which is a good candidate for high voltage applications. But simulations show that its driving current, maximum available gain, unilateral power gain, and current gain are approximately low which limit its usage in some of other applications. So, more improvement in SOI MESFET characteristics is useful.

In this paper a novel structure has been proposed which includes two extra oxide layers (boxes) symmetrically located in the channel at both sides of gate metal and extended drift region into the buried oxide. It should be mentioned that in this paper, capitalized “BOX” stands for “buried oxide”, but “box” with small letters is used for the two additional oxide layers. The key idea of this structure is increasing the current density by extending the effective channel thickness beside increase in breakdown voltage by high resistance symmetric boxes.

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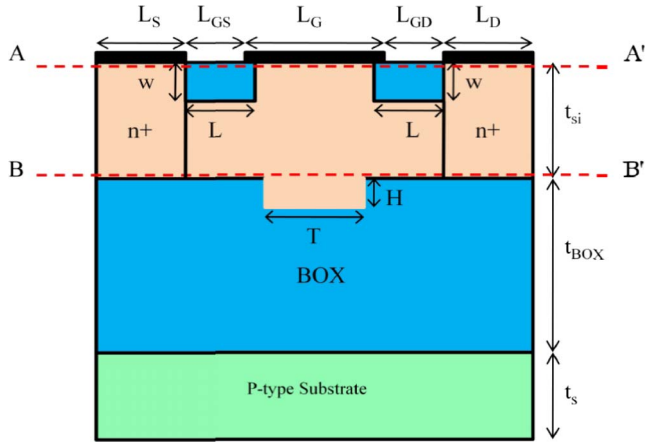

Fig. 1. Schematic view of SO-ED-SOI MESFET.

Table 1
Utilized parameters for the simulation of the structures.

Parameter	Symbol	Value
Length of source/drain	L_S/L_D	0.3 μm
Length of gate	L_G	0.5 μm
Space between gate and source/drain	L_{GS}/L_{GD}	0.5 μm
Thickness of silicon	t_{si}	0.2 μm
Thickness of buried oxide	t_{BOX}	0.4 μm
Thickness of substrate	t_S	0.1 μm
Doping of source/drain	N^+	10^{20} cm^{-3}
Doping of channel	N	10^{17} cm^{-3}
Doping of substrate	P	10^{17} cm^{-3}
Length of oxide parts	L	0.55 μm
Height of oxide parts	W	60 nm
Length of extended region	T	1.5 μm
Height of extended region	H	40 nm

Other achievements of this work include improvement in the cut-off frequency, unilateral power gain, maximum available gain, and current gain. In most of MESFET structures usually there is a trade-off between breakdown voltage and drain current which prevents increasing both parameters simultaneously. The power density in MESFET structures is limited due to the potential tradeoff between extra growth of breakdown voltage and drain current for a fixed device width. Reaching a large breakdown voltage requires small product of channel thickness and doping, which, nevertheless, will reduce the driving current, and vice versa. This paper -suggests a symmetric novel structure which improves both the breakdown voltage and drain current. In fact, meanwhile we have the increase in the breakdown voltage, drain current experiences higher values. To present our proposed structure, the simulation approach and required data for simulation are mentioned in Section 2. The 3rd section represents the simulation results that have been obtained using SILVACO ATLAS simulator [25]. A proposed process flow for fabricating this structure is discussed in Section 4. The final part is the conclusion section in which achievements of the paper are briefly mentioned.

2. Proposed structure and simulation method

Fig. 1 shows a schematic view of the structure which is proposed in this paper. In comparison with the conventional SOI MESFET, there are two additional oxide layers, and also the buried oxide shape is changed. The additional oxide layers are located in the channel at gate edges, and are made of SiO_2, the material used in fabricating SOI and bulk devices. The influence of these layers on the device performance will be discussed in the next sections. The proposed structure is symmetric. Symmetric structures are of interest in VLSI circuits. Main parameters required for simulating the structure, including device dimensions and

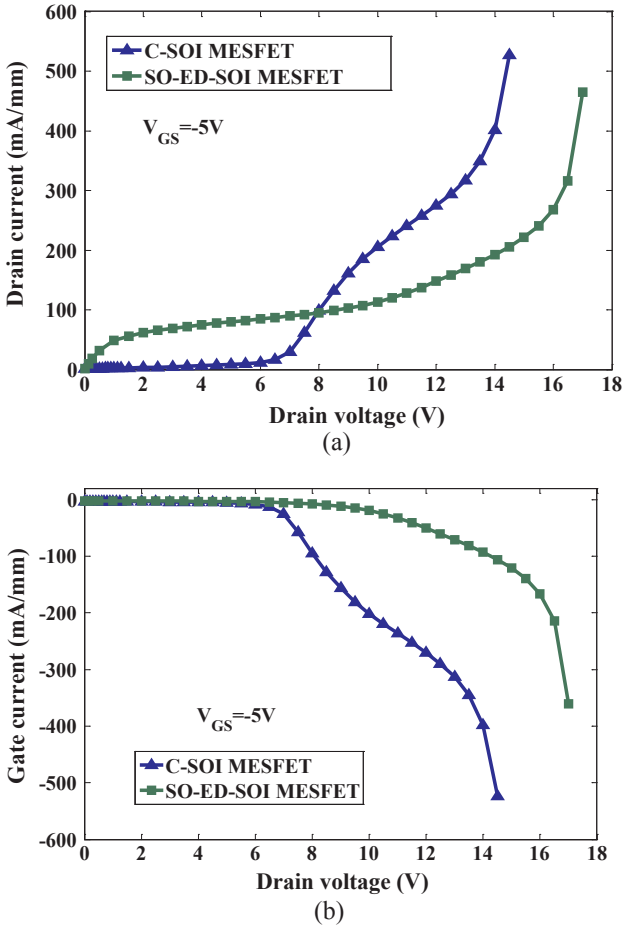

Fig. 2. Breakdown characteristics for drain current (a) and gate current (b) of C-SOI MESFET and SO-ED-SOI MESFET at $V_{GS} = -5$ V.

doping levels are listed in Table 1. In order to accurately compare the two structures (SO-ED-SOI MESFET and C-SOI MESFET), all common parameters are considered equal for both structures. The dimensions of additional oxide parts and the extended drift region (i.e. *W*, *L*, *T*, and H) have been determined after several simulations among different values for these parameters. The mentioned values for *W*, *L*, *T*, and H in Table 1, are the values which result in proper values for device high voltage and RF parameters. In this paper 2-D ATLAS simulator from SILVACO [25] has been utilized for simulations. ATLAS provides general capabilities for physically-based simulation of semiconductor devices and contains several physical models. Physical models employed in our simulations include: impact ionization (impact Selb model), Band-to-Band standard tunneling model (BBT.STD), parallel electric field-dependent mobility (Fldmob model), and incomplete ionization (incomplete model) concentration and temperature dependent mobility (analytic model), Shockley-Read-Hall (SRH) and Auger carrier generation/recombination models, and Lombardi mobility (CVT Model). It is worth mentioning that the simulator has been calibrated with the experimental data [26] to get realistic results. The results of comparison between experimental data and simulation is same as those have been mentioned in [24] which shows a good agreement between them.

3. Simulation results and discussions

As mentioned before, the difference between the proposed structure and its conventional counterpart is in two oxide layers in the channel at the edges of the gate, and also an extended drift region created in the middle of the buried oxide of the proposed structure. These differences have considerable effects on the electric performance of the device

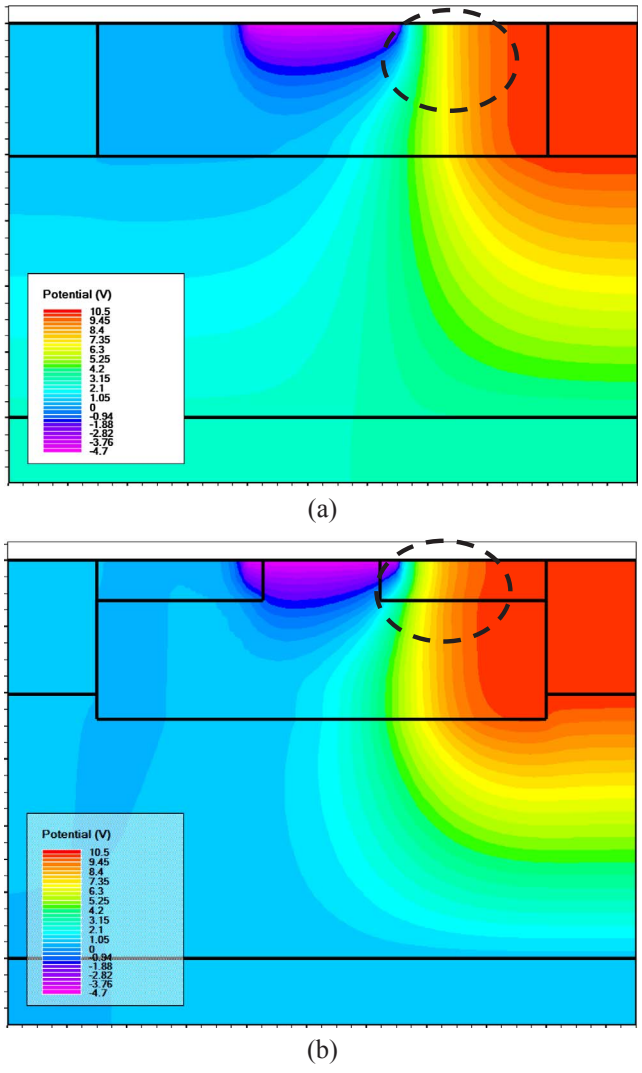

Fig. 3. Equi-potential contours of C-SOI MESFET (a) and SO-ED-SOI MESFET (b) at $V_{GS} = -5$ V and $V_{DS} = 10$.

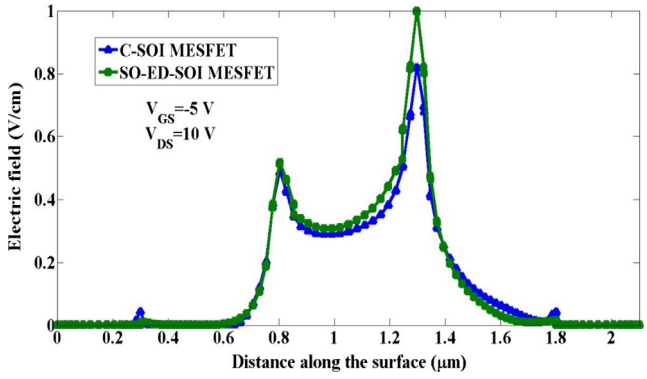

Fig. 4. Electric field of C-SOI MESFET and SO-ED-SOI MESFET along AA' cutline.

which are presented and discussed in this section. Fig. 2 illustrates breakdown characteristics of the devices. The current of gate-source and drain-source terminals at high drain voltages have been plotted to investigate the breakdown voltage. The breakdown voltage of SO-ED-SOI MESFET is higher than the breakdown voltage of C-SOI MESFET. At $V_{GS} = -5$V, it is ~6.1 V for SO-ED-SOI MESFET while it is ~3.5 V for the conventional structure. The additional oxide layer inserted in the channel between gate and drain affects breakdown voltage by

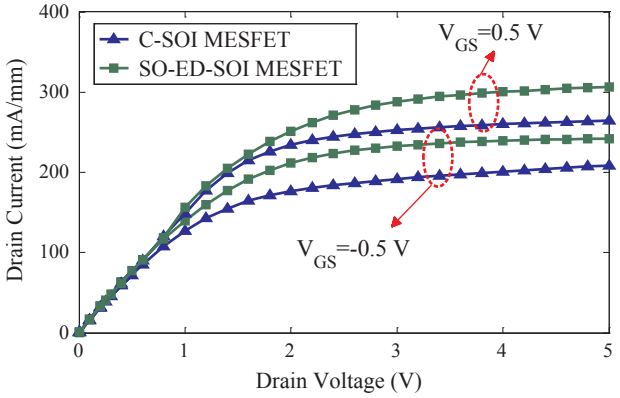

Fig. 5. Drain current of C-SOI MESFET and SO-ED-SOI MESFET at $V_{GS} = -0.5$ V and $V_{GS} = 0.5$ V.

increasing the critical electric field. It is located exactly in the region of the device where the electric field has maximum value and breakdown phenomenon starts from. In conventional structure, silicon is used in this area. When the internal electric field of the device reaches to the value of material critical electric field, the transistor breakdown is started. So where the critical electric field has a higher value, the device can tolerate a higher voltage before breaking down. SiO_2 has a higher critical electric field than Si, so SO-ED structure increases the breakdown voltage of the device by adding a layer of SiO_2 in the channel between gate and drain regions.

In Fig. 2, it seems that conventional structure is at pinch off for low values of drain voltage. It should be mentioned that where the gate source voltage is reduced (toward negative values), the current is reduced due to the deeper depletion region in the channel. The extended drift region in our proposed structure increases the effective channel width and consequently increases the device current. In Fig. 2, for conventional structure the channel is not completely in pinch off state at low drain-source voltages and there is still current in the channel but its value is considerably less than that of in proposed structure. For example at $V_D = 5$ V, the current for proposed structure is about 90 mA/mm while for conventional structure is about 9 mA/mm thus it is not recognizable in Fig. 2.

As noted before, the critical electric field of SiO_2 is higher than that of Si so, it can tolerate higher voltages. Fig. 3 shows the 2-D distribution of equi-potential contours for both structures. It shows that equi-potential lines are more concentrated in SO-ED structure. It means that the electric field is higher in SO-ED-SOI structure than C-SOI structure. Electric field is derivative of potential contours and the more concentrated potential lines, the higher electric fields. Also Fig. 4 shows the electric field values of both structures at $V_{GS} = -5$ V and $V_{DS} = 10$ V along AA' cutline shown in Fig. 1. The peak value of electric field is higher for SO-ED-SOI structure compared to conventional structure by about 20%. The maximum electric field value occurs below the gate metal at its right corner. If the peak (maximum) value of the electric field is higher for a device, it is expected to break at lower voltages. Here, maximum value of electric field of SO-ED SOI structure is higher than that of C-SOI structure, so it is expected that breakdown voltage of SO-ED SOI structure would be lower than breakdown voltage of C-SOI structure. But simulation results show the opposite. The reason of this increase in breakdown voltage is that the SiO_2 box used in the proposed structure, where the electric field reaches its maximum value, has the ability to tolerate higher electric fields than Si in conventional structure. In other words it has a higher critical electric field. Critical electric field is the maximum magnitude of electric fields which the material can tolerate without breaking down. The critical electric field for Si in conventional structure is about 0.3 MV/cm while for SiO_2 in proposed structure is about 10 MV/cm [24] which shows more than 300 times higher value for the latter. This means that the proposed structure not

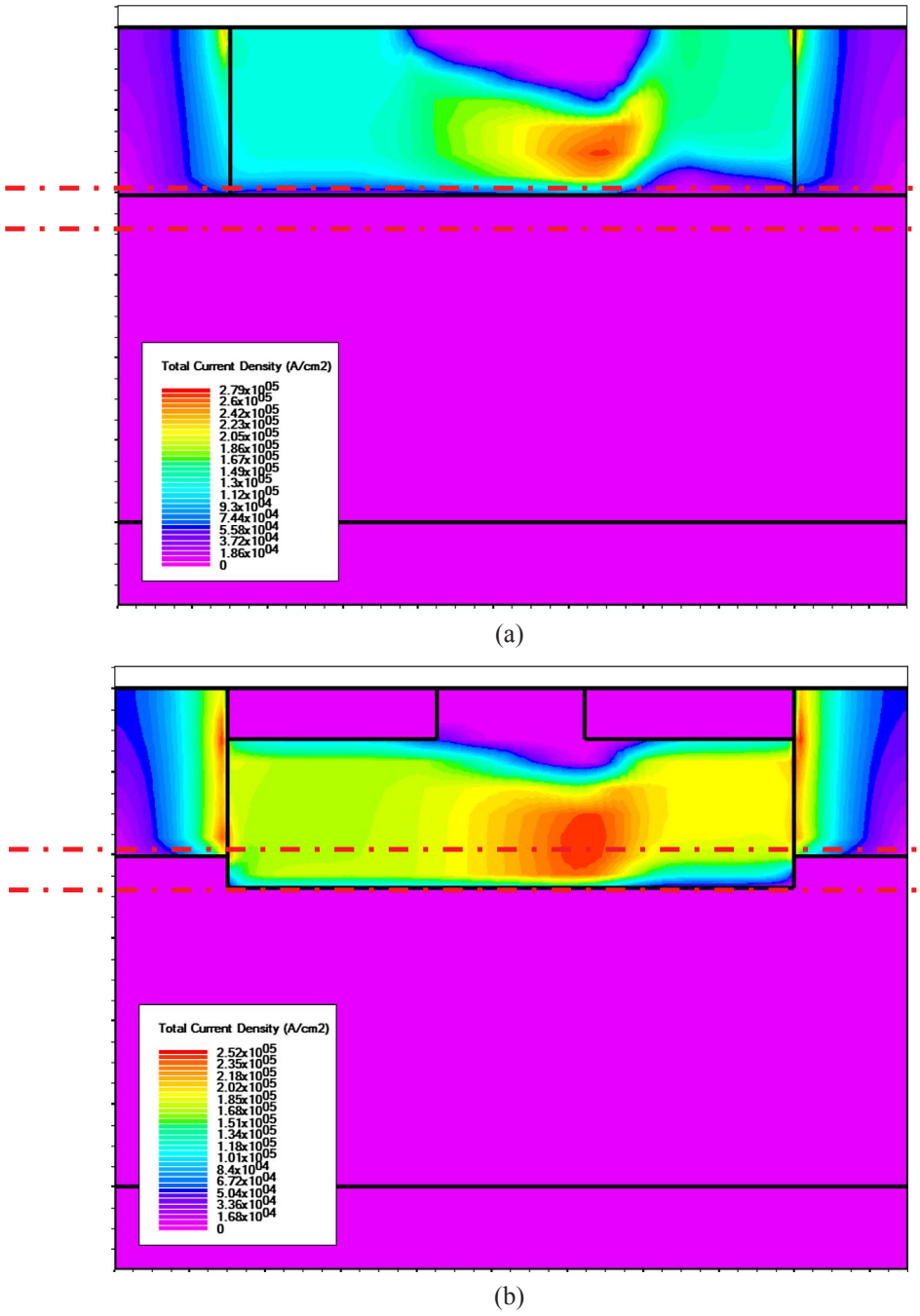

Fig. 6. Total current density of C-SOI MESFET (a) and SO-ED-SOI MESFET (b) at V_{GS} = 0.5 V and V_{DS} = 5.

only tolerates this 20 percent larger electric field but also is ableto accept higher values.

Another considerable feature of the proposed structure is its higher drain current in comparison with conventional structure. This is clearly shown in Fig. 5 where the drain current of C-SOI structure and SO-ED-SOI structure are illustrated at the applied biases of $V_{GS} = -0.5$ V and $V_{GS} = 0.5$ V. This achievement has been realized by change in buried oxide and drift region. The extended drift region toward buried oxide is filled by *n*-type silicon with the same doping level as the channel. In fact this region extends the channel and increases the total current density by providing more space for carriers to pass (i.e. wider effective channel thickness). In other words, the proposed structure facilitates the current flow through the channel. In Fig. 6, total current density of C-SOI and SO-ED-SOI structures are shown at the applied bias of $V_{GS} = 0.5$ V and $V_{DS} = 5$V. As noted in the figure, purple colored parts show zero current density and as it is clear, such parts are much smaller in the channel region of SO-ED-SOI. The extended drift region between

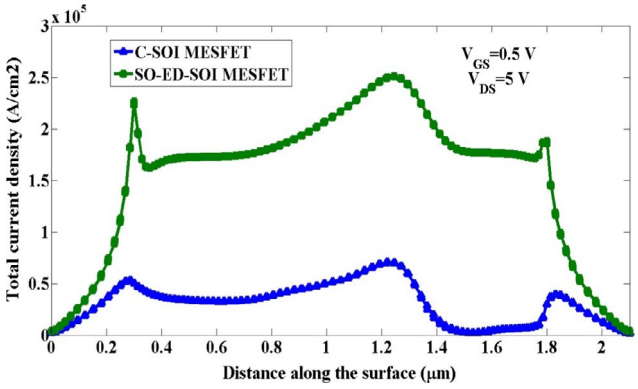

Fig. 7. Total current density of C-SOI MESFET and SO-ED-SOI MESFET along BB' cutline.

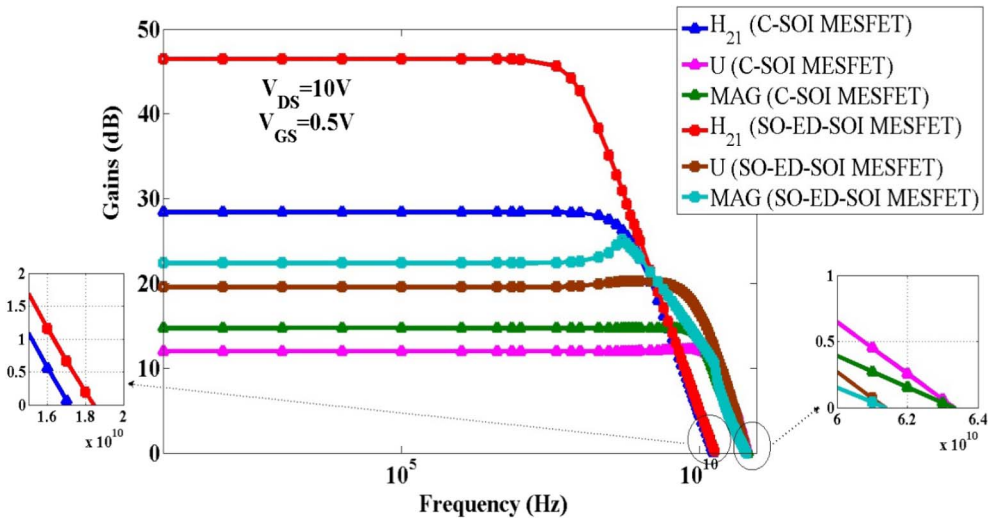

Fig. 8. H_{21}, U and MAG as functions of frequency for C-SOI MESFET and SO-ED-SOI MESFET.

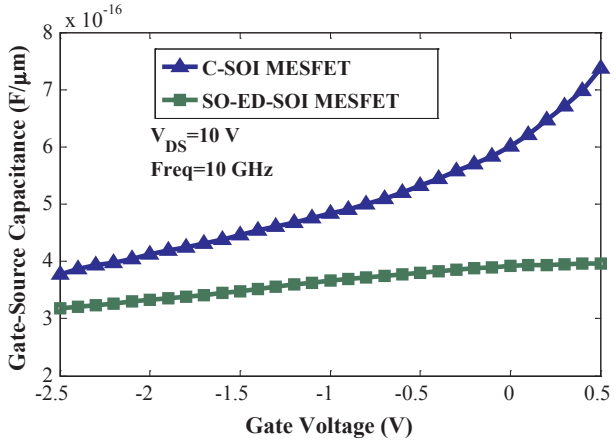

Fig. 9. Gate-source capacitance versus gate-source voltage for C-SOI MESFET and SO-ED-SOI MESFET.

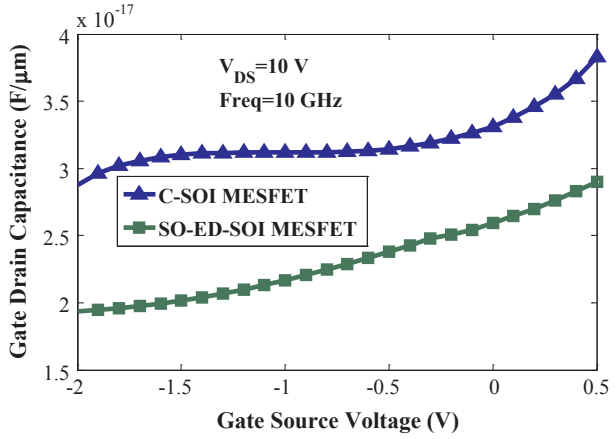

Fig. 10. Gate-drain capacitance versus gate-source voltage for C-SOI MESFET and SO-ED-SOI MESFET.

parallel dash-lines shown in SO-ED structure contains considerable portion of current density. The equivalent region in conventional structure fabricated mostly by buried oxide which cannot transmit significant current density. Quantified total current density is also illustrated in Fig. 7 for better insight. This figure shows a noticeable increase in the total current density of the proposed structure. This plot has been obtained along the horizontal cutline BB' shown in Fig. 1 at the applied bias of V_{GS} = 0.5 V and V_{DS} = 5 V. As the region between dash-lines of Fig. 6 shows, the effective channel thickness increases. An increase in channel thickness reduces the channel resistance according to the below equation [27]:

$$R = \frac{\rho \times L_G}{Z \times h(x)} \quad (1)$$

where h(x) is channel thickness, ρ is resistivity, and Z is its width. Also as mentioned in Table 1, L_G is gate length. Thus, by decreasing the channel resistance, I_D is increased. Simultaneous increase in breakdown voltage and output current is a valuable feature for the proposed structure. It should be mentioned that maximum output power density (P_{max}) depends on breakdown voltage and driving current [27]. As stated above, both of these parameters are enhanced by SO-ED structure and consequently P_{max} is improved, too.

SO-ED structure also improves the hot carrier effect. As we mentioned before, the maximum electric field in conventional structure occurs in Si material while for proposed structure occurs in SiO_2. The critical electric field in SiO_2 is larger than that of Si and SO-ED structure can tolerate higher electric field than conventional structure. In spite of 20% higher electric field (Fig. 4), insertion of an oxide layer in the place where the electric field gets its maximum value, helps the reduction in hot carrier effect. As Fig. 6 shows, creation of SiO_2 box prevents the channel carriers to pass through the place where the electric field is maximum so, governing enough electric field for hot electron

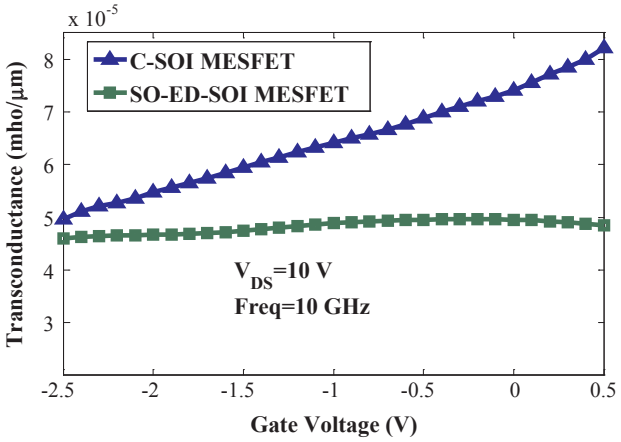

Fig. 11. Transconductance (gm) versus gate-source voltage for C-SOI MESFET and SO-ED-SOI MESFET.

Table 2
The comparison among DCR [23], POML [24], and SO-ED structure.

	Breakdown voltage	f_t	f_{max}	Current	U	MAG	H_{21}
	$V_{GS} = -5$ V	$V_{GS} = 0$ V	$V_{GS} = 0$ V	$V_{GS} = 0.5$ V	$V_{GS} = 0$ V	$V_{GS} = 0$ V	$V_{GS} = 0$ V
				$V_{DS} = 5$ V	$V_{DS} = 10$ V	$V_{DS} = 10$ V	$V_{DS} = 10$ V
POML [24]	29.5 V	18.3 GHz	92.5 GHz	210 mA/mm	8 dB	9 dB	21 dB
DCR [23]	14.5 V	16.5 GHz	59.2 GHz	228 mA/mm	8.7 dB	13.1 dB	38 dB
SO-ED [This work]	16.1 V	18.5 GHz	65.2 GHz	300 mA/mm	12 dB	14 dB	34 dB

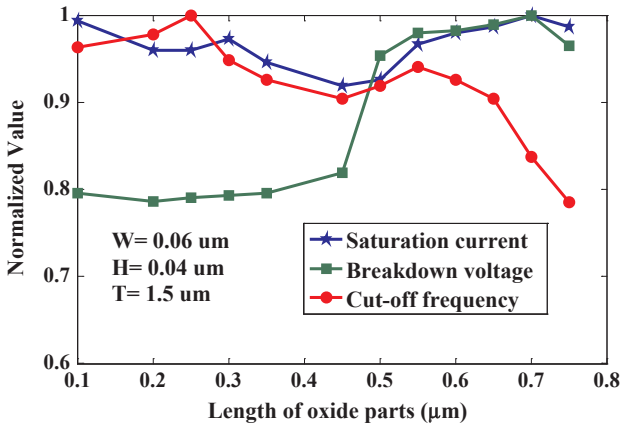

Fig. 12. Optimization process for length of oxide part.

phenomena is harder in our proposed structure compared to conventional structure.

Simulations show that the oxide part located in the channel between gate and source impacts RF characteristics of the device. Unilateral power gain (U), current gain (H_{21}) and maximum available gain (MAG) of C-SOI MESFET and SO-ED-SOI MESFET are shown as functions of frequency in Fig. 8. Cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) can be extracted from this plot. The f_t is the frequency where H_{21} reaches zero dB, and f_{max} is the frequency at which U gets zero dB. By these definitions, f_t of C-SOI MESFET is 17.5 GHz while it is increased to 18.4 GHz in SO-ED-SOI MESFET. f_{max} is 63.4 GHz for the C-SOI MESFET but it lowers to 61.3 GHz for the SO-ED-SOI MESFET. Also, this figure obviously shows that H_{21}, U and MAG have higher values for the SO-ED-SOI MESFET all over the flat band frequency range. A trivial decrease in f_{max} of the proposed structure can be neglected in presence of about 63% increase in its unilateral power gain at flat band frequencies. Also, in flat part of plots, H_{21} and MAG shows 63.5% and 52% higher values by applying SO-ED structure. The expression to calculate f_t is as follows [28]:

$$f_t = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{2}$$

As it is clear, gate-source and gate-drain capacitances influence f_t and if they are lower for a device, f_t would be higher. The increment of f_t is due to adding oxide regions and decreasing the capacitances between gate and drain/source regions. C_{GS} and C_{GD} versus gate-source voltage for both C-SOI and SO-ED-SOI structures are shown in Figs. 9 and 10, respectively. Also, Fig. 11 shows transconductance (gm) variation by gate voltage. They are calculated at $f = 10$ GHz and $V_{DS} = 10$ V. The Figs. 10 and 11 show an obvious decrease in the C_{GS} and C_{GD} by applying the proposed structure. The oxide layers operate as a useful obstacle in extending the depletion region beneath the gate into the drift region thus decreasing the coupling between gate and drain/source. Each oxide box lowers its relevant gate capacitance. The source side box lowers the gate-source capacitance and the drain side oxide reduces the gate-drain capacitance. Also, a reduction in gm can be observed in Fig. 11. Figs. 9–11 show that gate-source capacitance, gate-drain capacitance, and transconductance all are reduced in our proposed structure compared to conventional structure. Reduction in capacitances increases the cut-off frequency while reduction in gm decreases its value. Simulations prove that the former dominates the latter and consequently the ft increases.

Lower device capacitances leads to higher cut-off frequency and therefore better performance of the device. The reduction of f_{max} for the SO-ED-SOI MESFET in comparison with the C-SOI MESFET can be explained by the following expression [27]:

$$f_{\max} = \frac{f_t}{2}\sqrt{\frac{R_{DS}}{R_G}} \tag{3}$$

The expression reveals that f_{max} depends on f_t and R_{DS}/R_G ratio where R_{DS} is the drain-source resistance and R_G is the gate resistance. As noted before, drain current of SO-ED-SOI MESFET is higher than that of C-SOI MESFET so R_{DS} and therefore R_{DS}/R_G ratio are lower for SO-ED-SOI MESFET. Thus the device experiences small reduction in f_{max}. This slight reduction doesn't have severe effects on proposed device performance due to considerable improvement in current, breakdown voltage and also considering improvement in cut-off frequency, H_{21}, U and MAG.

Table 2 shows the results of comparison with recently reported works, DCR SOI MESFET [23], and POML SOI MESFET [24]. To compare the structures at fair conditions, biasing and physical parameters should be the same. It means that the device dimensions, bias points and activated models in simulator should be the same for both structures. To do so, we simulate SO-ED and DCR structures with conditions mentioned in [24] and the results declared in Table 2 to compare SO-ED, DCR and POML structures in fair conditions. It can be seen that POML structure has brilliant breakdown voltage and maximum oscillation frequency. But SO-ED structure outperforms POML structure in other parameters such as driving current, unilateral power gain, maximum available gain, and current gain. It means that however POML structure improves f_{max}, but other AC parameters such as U, MAG, and H_{21} are lower than SO-ED structure. Another advantage of SO-ED is its symmetrical structure while POML structure is asymmetrical. In fabrication process and for circuit designers the symmetrical structure is more desired. DCR structure is similar to SO-ED structure which uses two p-type boxes at both sides of gate metal. Its improvement mechanism is based on electric field reduction in gate metal corner [23] while our proposed structure works based on using boxes with higher critical electric field. The results show that, neglecting a small reduction in H_{21}, SO-ED structure outperforms DCR structure in investigated parameters.

As mentioned in introduction, the dimensions of boxes and the extended drift region (W, L, T, and H) have been determined after several simulations among different values for these parameters. In fact we have four optimization steps to find the proper values for W, L, T, and

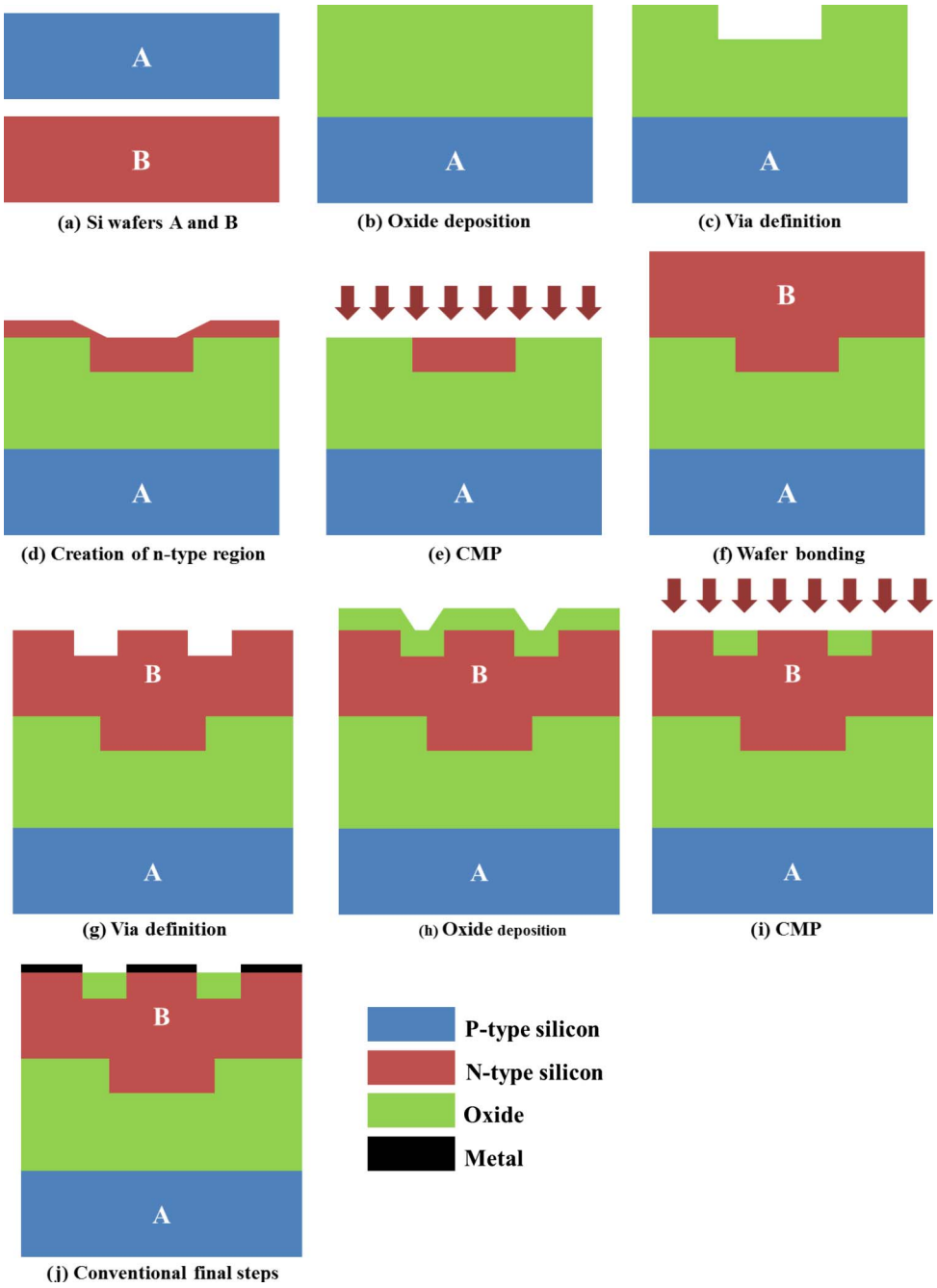

Fig. 13. (a) to (j) Fabrication process of SO-ED-SOI MESFET.

H. To do that, in each step one of these parameters has been varied while the other were fixed. After finding the best value for varied dimension, this value is fixed in next steps. This process is repeated to obtain all four parameters. Breakdown voltage, cut-off frequency, and device saturation current have been considered as evaluation characteristics. In Fig. 12, the optimization process has been illustrated for length of oxide part (L). It can be seen that a length between 0.5 μm and 0.6 μm can be considered as a proper length so, we selected 0.55 μm for box length. Other parameters, including W, T, and H, have been obtained with similar process.

4. Proposed process flow for fabrication of SO-ED-SOI MESFET structure

As shown in Fig. 13(a), a *P*-type ⟨1 0 0⟩ oriented silicon wafer A and an *N*-type ⟨1 0 0⟩ oriented silicon wafer B are required. Then oxide deposition is done on wafer A which will role as the device substrate, in order to form the buried oxide of the device (Fig. 13(b)). The next step is via definition on the oxide in order to form the lower-level n-region (Fig. 13(c)). The deposition of Si and then ion implantation of donor material can be used to create the n-type region in (Fig. 13(d)). Then chemical mechanical planarization (CMP) should be done in order to clean the device surface from additional particles remained from the last step (Fig. 13(e)). The next step is bonding the other wafer (B) which will role as the active layer of the structure on the other part (Fig. 13(f)). Then via definition is done as shown in Fig. 13(g). After that, oxide will be deposed on the device to fill the regions created at the previous step and form the two oxide parts of the structure (Fig. 13(h)). At the next step, CMP will be done to remove the additional oxide particles on the device (Fig. 13(i)). Finally conventional

steps are done in order to complete the fabrication process in Fig. 13(j). It should be mentioned that Cu has been used as gate, drain, and source metal. From above steps it is obvious that fabrication of the proposed structure is convenient and includes usual steps used in basic device fabrication. There is also another method for fabricating SOI devices which is named “smart-cut method”. This method is based on hydrogen implantation and wafer bonding [29].

5. Conclusion

A novel structure for SOI MESFET has been proposed in this paper. This symmetric structure contains two oxide parts in the channel. Also a part of its buried oxide is replaced by *n*-type silicon. Neglecting a small reduction in maximum oscillation frequency, the advantages of SO-ED-SOI MESFET over C-SOI MESFET are briefly listed below:

- Cut-off frequency is raised from 17.5 GHz in conventional to 18.4 GHz in the proposed structure because of the existence of oxide layers in the channel between gate -source and gate-drain.
- Breakdown voltage of C-SOI MESFET is 13.5 V and is increased to 16.1 V in SO-ED-SOI MESFET due to locating an oxide layer in the channel between gate and drain which has a higher critical electric field than silicon so it can tolerate higher drain voltages than C-SOI MESFET.
- Increase in drain current is obtained due to widening the channel region by extending the drift region into the buried oxide.
- Simultaneous increase in current and breakdown voltage is achieved.
- Gate capacitances are reduced in the SO-ED-SOI MESFET because of locating the oxide layers which reduce the capacitive coupling between gate and source, and gate and drain regions.
- Maximum output power density of the device is improved.
- Unilateral power gain, maximum available gain and current gain are enhanced by 63, 52 and 63.5% respectively.

All the obtained results show that the proposed structure has reached a capability to improve the electrical performance, successfully. Therefore, it can be considered as better-quality structure to replace the conventional SOI MESFET.

Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.aeue.2018.01.001.

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